IN THE CLAIMS:

Please amend the claims as follows:

33. (Currently Amended) A semiconductor device comprising:

inputting means for inputting a logical address;

converting means for converting the logical address into a physical address;

a plurality of multilevel memory cells arranged so as to correspond to physical addresses, each cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more;

controlling means for selecting one of the cells corresponding to the physical address and designating one of the data components in accordance with the logical address; and

outputting means for outputting the designated data component [[,]];

wherein the semiconductor device has a judging value for specifying, by one-time specifying operation, at least one of the data components[[,]]; and

wherein when the logical address is included in an address space Al that corresponds to an address space including the physical address, the controlling means specifies the designated data component by means of the judging value, thus the specified data being output by the outputting means.

34. (Currently Amended) The semiconductor device according to claim 33;

wherein each cell stores 2^n levels of data each expressed by data components (X1, X2, ..., Xn) of n - th dimension ($n \geq 2$)[[,]];

wherein the semiconductor device ~~having~~ has a first judging value for specifying, by one-time specifying operation, at least the data component Xl having data of the logical address included in the address space Al, when the logical address included in the address space Al is input by the inputting means, the data component X1 specified by the controlling means by means of the first judging value is output by the outputting means among the data components stored in the cell corresponding to the logical address included in the address space Al.

35. (Currently Amended) The semiconductor device according to claim 34, having judging values for specifying the data components (X2, ..., Xn) of a logical address included in address spaces (A2, ..., An) close to the address space Al, wherein the data components (X2, ..., Xn) have the data stored sequentially in the order of closeness to the address space Al[[,]];

wherein the controlling means specifies a data component Xk (k = 1, 2, ..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including the logical address input by the inputting means, thus the data component Xk being output by the outputting means.

36. (Original) The semiconductor device according to claim 33, wherein each cell is provided with a control gate and a charge accumulating layer having a floating gate.